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WHAT IS CLAIMED IS:

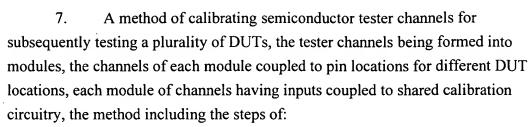
- 1. Automatic test equipment for testing a plurality of devices-under-test, each of the devices-under-test having a predetermined number of input/output contact points for receiving and outputting signals, said automatic test equipment including:

 a plurality of channel modules, each of the channel modules having a plurality of channels, each channel corresponding to one of the contact points; and programmable delay circuitry coupled to each channel module, the programmable delay circuitry including a deskew circuit shared by more than one of the channels of the coupled channel module.
- 2. Automatic test equipment according to claim 1 wherein:
 each channel module comprises an integrated circuit formed with more
 than one channel.
- 3. A method of calibrating channels of a parallel tester having calibration circuitry shared with tester channels, the method including the steps of:

 determining the level of accuracy required from the calibration circuitry to calibrate the channels;

collecting deskew data for the channels; optimizing the collected deskew data; and storing the deskew data.

- 4. A method of calibrating channels of a parallel tester according to claim3 wherein said optimizing step includes:averaging the deskew data from more than one channel.
- 5. A method of calibrating channels of a parallel tester according to claim3 wherein said optimizing step includes:averaging the deskew data from all of the channels in parallel.
- 6. A method of calibrating channels of a parallel tester according to claim3 wherein said optimizing step includes:utilizing the individual deskew data for each channel.



selecting a set of DUT locations;

identifying each tester channel from each module coupled to the selected DUT locations;

collecting deskew data for each of the identified channels with the shared deskew circuitry;

optimizing the collected deskew data;

storing the optimized deskew data for use during device testing; and continuing the selecting, identifying, collecting, optimizing and storing steps until all of the tester channels are calibrated.

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8. A method of calibrating semiconductor tester channels according to claim 7 wherein:

the optimizing step includes averaging the collected deskew data for groups of channels.

9. A method of calibrating semiconductor tester channels according to claim 7 wherein:

the optimizing step includes using the collected deskew data as the calibration data for each channel.

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10. A method of testing a plurality of DUTs with a semiconductor tester, the tester including a plurality of channels formed into modules, the channels of each module coupled to pins of different DUTs, each module of channels having inputs coupled to a shared programmable delay circuit, the method including the steps of:

selecting a group of DUTs to test;

identifying the channels from each module coupled to each pin of the selected DUTs;

loading optimized calibration data for the identified channels into the programmable delay circuit;

testing the selected DUTs; and

continuing the selecting, identifying, loading and testing steps until all of the DUTs are tested.